REMARKS

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-6 and 13-24 are all of the claims pending in the present Application. New claims 14-24 are added. Claims 1-4 and 13 stand rejected under 35 USC §102(e) as being anticipated by US Patent No. 6,265,739 to Yaegashi et al. Claims 5 and 6 stand rejected under 35 USC §103(a) as unpatentable over Yaegashi, further in view of US Patent 5,824,584 to Chen et al.

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As disclosed and claimed, for example by independent claim 1, the present invention is directed to a method of forming a semiconductor memory device capable of electrically writing and erasing data. The device includes a plurality of cell transistors for storing data, each cell transistor having a floating gate electrode and a control gate electrode, and a plurality of select transistors for controlling and selecting the cell transistors.

A key feature of the inventive method is that, before the control gate electrodes of the cell transistors are formed, the surface of a substrate directly above channel regions of the select transistors, fabricated in the same process as the cell transistors, is exposed, and gate insulating films of the select transistors are formed on the exposed surface of the substrate. The control gate electrodes of the cell transistors are formed, and gate electrodes of the select transistors are formed on the gate insulating films.

The advantage of the present invention is that the number of fabrication steps is reduced, as compared to the conventional methods.

II. THE PRIOR ART REJECTION

The Examiner asserts that US Patent No. 6,265,739 to Yaegashi et al. anticipates the invention as described by claims 1-4 and 13, and in combination with US Patent 5,824,584 to Chen et al., renders claims 5 and 6 as unpatentable.

Applicant gratefully acknowledges the Examiner's explaining how he inteprets the claim language "... *before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above channel regions of said select transistors* ...."

According to the Examiner, this above-cited phrase from claim 1 "... may be reasonably interpreted to mean the step as being the cleaning step performed in all wafer fabrication before any processing step occurs which takes place before the control gate electrodes are formed to expose the substrate in the same process as the cell transistors."

Applicant believes that the original wording is adequate to distinguish from the Examiner's interpretation, since a wafer undergoing an initial cleaning process does not have any channel regions yet formed. Therefore, Applicant believes that the Examiner's broad interpretation would not have beeen reasonable to one of ordinary skill in the art.

However, in order to expedite prosecution, Applicant has amended claim 1 to further clarify the invention for the benefit of the Examiner.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "... *forming a channel region for each said cell transistor; before forming the control gate electrodes of said cell transistors, exposing a surface of a substrate directly above said channel regions of said select transistors fabricated in the same process as the cell transistors* ...."

For this reason, the claimed invention is fully patentable over Yaegashi.

The Chen reference was introduced to demonstrate the gate insulation thickness over peripheal circuit transistors and does not overcome the deficiency identified above for Yaegashi.

Further, the other prior art of record has been reviewed, but it too, even in combination with Yaegashi and Chen, fails to teach or suggest the claimed invention.

III. FORMAL MATTERS AND CONCLUSION

Applicant submits that claims 1-6 and 13-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 7/24/03

Frederick E. Cooperrider
Reg. No. 36,769

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254